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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,516	07/29/2003	David W. Hansquine	030192	7900

7590 11/02/2006

QUALCOMM Incorporated
Attn: Patent Department
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EXAMINER	
BARAN, MARY C	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,516	HANSQUINE ET AL.	
	Examiner	Art Unit	
	Mary Kate B. Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 5-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3 and 5-24* is/are allowed.

6)☒ Claim(s) *25-31* is/are rejected.

7)☒ Claim(s) *32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The action is responsive to the Amendment filed on 9 August 2006. Claims 3 and 5-32 are pending. Claims 6-8, 10, 14, 16-19 and 22-27 are amended. Claims 1, 2 and 4 are cancelled.

2. The amendments filed 9 August 2006 are sufficient to overcome the prior objections to the claims.

Claim Objections

3. Claim 32 is objected to because of the following informalities: claim 32 is dependent on cancelled claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Crouch et al. (U.S. Patent No. 5,617,531) (hereinafter Crouch '531).

Referring to claim 25, Crouch '531 teaches a device comprising: first-level built-in self-test (BIST) means for issuing commands that define a BIST algorithm for a plurality of distributed memory modules having different timing requirements (see Crouch '531, column 8 line 66 – column 9 line 14) and physical characteristics (see Crouch '531, column 5 lines 7-12); second-level BIST means for processing the commands to generate sequences of memory operations (see Crouch '531, column 7 lines 14-24) in accordance with the timing requirements of the memory modules (see Crouch '531, column 9 lines 6-13); and third-level BIST means for generating translated address and data signals from the memory operations based on the physical characteristics of the memory modules to apply the BIST algorithm to the distributed memory modules (see Crouch '531, column 7 line 62 – column 8 line 48).

Referring to claim 27, Crouch '531 teaches a method comprising: issuing commands from a centralized BIST controller to a sequencer, wherein the commands define a memory test algorithm to be applied to a set of distributed memory modules without regard to physical characteristics or timing requirements of the memory modules (see Crouch '531, column 7 line 62 – column 8 line 16); processing the commands with the sequencer to generate one or more sequencers of memory operations (see Crouch '531, column 7 lines 14-24) in accordance with the timing requirements of the memory modules (see Crouch '531, column 9 lines 6-13); and applying the memory operations to the distributed memory modules to test the memory modules (see Crouch '531, column 8 lines 17-18).

Referring to claim 28, Crouch '531 teaches translating address and data signals associated with the memory operations with memory interfaces coupled to each of the memory modules to generate translated address and data signals based on the physical characteristics of each of the memory modules, and wherein applying the memory operations comprises applying the translated address and data signals to test the memory modules (see Crouch '531, column 7 line 62 – column 8 line 16).

Referring to claim 29, Crouch '531 teaches selecting the memory test algorithm from one of a plurality of memory test algorithms stored within an algorithm memory (see Crouch '531, column 8 lines 17-48).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Crouch et al. (U.S. Patent No. 5,617,531) (hereinafter Crouch '531) in view of Crouch et al. (U.S. Patent No. 5,995,731) (hereinafter Crouch '731).

Referring to claim 26, Crouch '531 teaches all the features of the claimed invention except an algorithm memory that stores the set of commands as one of a set

of selectable memory test algorithms having associated commands; and an algorithm controller to retrieve the commands from the algorithm memory and issue the commands associated with the selected memory test algorithm to the sequencer; wherein the algorithm controller issues each of the commands to the sequencers in parallel for application to the respective subsets of the memory interfaces.

Crouch '731 teaches an algorithm memory that stores the set of commands as one of a set of selectable memory test algorithms having associated commands (see Crouch '731, column 6 lines 10-18); and an algorithm controller to retrieve the commands from the algorithm memory and issue the commands associated with the selected memory test algorithm to the sequencer (see Crouch '731, column 6 lines 18-22); wherein the algorithm controller issues each of the commands to the sequencers in parallel for application to the respective subsets of the memory interfaces (see Crouch '731, column 7 line 56 – column 8 line 3).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch '531 to include the teachings of Crouch '731 because storing and issuing a set of algorithms for memory testing would have allowed the skilled artisan to select a specific test for maximum fault detection.

6. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crouch et al. (U.S. Patent No. 5,617,531) (hereinafter Crouch '531) in vies of Crouch et al. (U.S. Patent No. 5,995,731) (hereinafter Crouch '731) and in further view of Johnston et al. (U.S. Patent No. 6,272,588) (hereinafter Johnston).

Referring to claim 30, Crouch '531 and Crouch '731 teach all the features of the claimed invention except translating address and data signals with memory interfaces based on at least one of a number of rows of the respective memory module, a number of columns of the respective memory module, and a number of row-column matrices of the respective memory module.

Johnston teaches translating address and data signals with memory interfaces based on at least one of a number of rows of the respective memory module and a number of columns of the respective memory module of the respective memory module (see Johnston, column 6 lines 1-14).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch '531 and Crouch '731 to include the teachings of Johnston because accounting for the rows or columns would have allowed the skilled artisan to easily incorporate the BIST into existing architecture (see Johnston, column 3 lines 13-19).

Referring to claim 31, Crouch '531 and Crouch '731 teach all the features of the claimed invention except issuing commands in accordance with a command protocol that defines a set of supported commands having operands and a set of parameters that define the memory operations to be generated by the sequencer.

Johnston teaches issuing commands in accordance with a command protocol that defines a set of supported commands having operands and a set of parameters

that define the memory operations to be generated by the sequencer (see Johnston, column 4 lines 40-53).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Crouch '531 and Crouch '731 to include the teachings of Johnston because having a command including an operand and a set of parameters would have allowed the skilled artisan to ensure that data is not lost over time by normal current leakage (see Johnston, column 4 lines 53-58).

Allowable Subject Matter

7. Claims 3 and 5-24 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter:

Claims 3 and 5-24 are allowable over the prior art because a system comprising: a plurality of sequencers, each sequencer coupled to a different subset of the memory modules is not found, taught or suggested in the prior art of record.

Response to Arguments

9. Applicant's arguments, with respect to claims 25-31, filed 9 August 2006 have been fully considered but they are not persuasive.

Applicant argues that Crouch '531 does not teach, "memory modules with different timing requirements"; however, Applicant's arguments are not well taken.

Crouch '531 teaches multiple memory modules 12-14 having two different timing requirements (i.e. time intervals) for sending and receiving data (see Crouch '531, column 8 line 66 – column 9 line 14). Therefore Crouch '531 teaches memory modules (see Crouch '531, Figure 1, Memory 12-14) with different timing requirements (see Crouch '531, column 8 line 66 – column 9 line 14).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B. Baran whose telephone number is (571) 272-2211. The examiner can normally be reached on Monday - Friday from 9:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

28 October 2006

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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